

## A MULTI-CHIP GaAs MONOLITHIC TRANSMIT/RECEIVE MODULE FOR X-BAND

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Abstract

The design, construction, and performance of an X-band multi-chip GaAs monolithic transmit/receive module is described. The module consists of a four-bit FET phase-shifter, two-stage low-noise amplifier, four-stage power amplifier, and associated FET switches.

Introduction

Monolithic microwave integrated circuits (MMICs) fabricated on GaAs substrates offer the potential for significant reductions in size, weight, and cost with increased reliability as compared with conventional hybrid integrated circuits. By monolithic we mean an approach wherein all active and passive components and interconnections are formed into or onto a semi-insulating substrate by some deposition scheme.

The advantages accruing from this approach are especially attractive in applications where electronically scanned active phased-array antennas are used. Such antennas consist of a two-dimensional array of closely-packed (about a half-wavelength in separation) transmit-receive modules. These modules individually phase-shift a transmitted or received signal in accordance with a sequence of command signals. By an appropriate control of the phase-shift of each module, the direction and shape of the transmitted or received antenna radiation pattern is determined. By introducing gain into the module, an active array is obtained.

A block diagram of an active transmit/receive module is shown in Fig. 1. As can be seen the module consists of a power amplifier (marked "transmitter"), low-noise small-signal amplifier (marked "receiver") and four single-pole, double-throw switches which control the direction of signal flow. A key element in the module is the phase shifter which, in addition to introducing a differential phase shift in the receive/transmit signal flow path, may also have gain. By an appropriate sequence of the settings of the SPDT switches  $s_1$  to  $s_4$  the module can be used to either amplify a source signal received from the "left" or a received signal coming from the "right". In either mode of operation,

the active phase-shifter is introduced into the signal path in the proper direction of signal flow by switches  $s_2$  and  $s_3$ .

We wish to describe in this paper, a preliminary (brassboard) module of eleven individual monolithic GaAs chips consisting of the four switches, four phase-shift bits, a two-stage low-noise amplifier, and a cascaded pair of two-stage power amplifiers. All of the monolithic chips are interconnected by appropriate microstrip lines printed on alumina substrates which are coplanar with the GaAs chips.

It should be pointed out that the alumina substrates, which contain 50-ohm microstrip lines only, are merely used to interconnect the GaAs chips. The GaAs chips contain, not only the appropriate rf circuitry and active elements (FETs), but in addition all of the bias circuitry.

Although this module is considered to be a multi-chip monolithic circuit, it is a convenient, intermediate stage leading eventually to a higher level of integration involving fewer chips. This transition to a higher level of integration is being carried out at our laboratory. It is appropriate to report on this multi-chip approach, since, to our knowledge, this complexity of monolithic integration has not been reported for any microwave circuit to date.

The Transmit/Receive Module

Figure 2 is a photograph of the transmit/receive module. The operating band is 9-10 GHz. Starting from the left, one may note the three monolithic switches,  $s_1$ ,  $s_2$ ,  $s_3$ , followed by four chips in a rectangular array which are the four bits of an active phase-shifter. Further to the right are two cascaded chips, each of which is a two-stage power amplifier, followed by another switch,  $s_4$ . The low-noise amplifier chip is at the lower right.

All eleven of the functional chips use FETs as the active element. The FETs are formed in epitaxial layers grown by the arsenic trichloride system on 0.1 mm

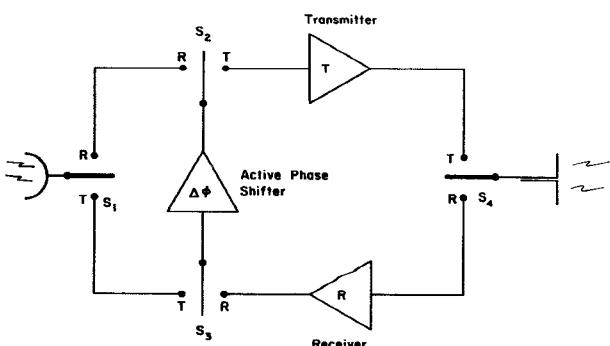


Fig. 1 Block diagram of an active transmit/receive module.

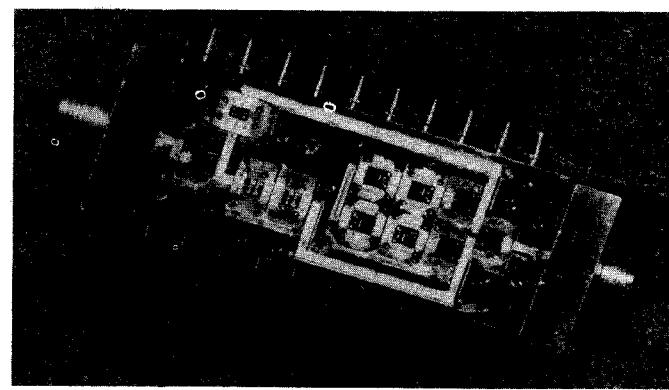


Fig. 2 Photograph of an assembled transmit/receive module.

thick semi-insulating GaAs substrates. These active elements are electrically separated by a combination of a partial etching and isolation implanting of the unused active epi-layer external to the device areas. All conductor metallization is gold, approximately 3 microns thick. The gate lengths of the FETs are all, nominally, one micron, except for the low-noise amplifier, for which gates 0.7 microns long were used. Both via hole grounding and air-bridge technologies were used.

#### Brief Description of Individual Chips

The low-noise and power amplifier circuits are of a conventional narrow-band design and their performances have been reported elsewhere.<sup>1,2</sup> Photographs of these two circuits in monolithic chip form are shown in Fig. 3 and 4, respectively.

The low-noise amplifier consists of two 150  $\mu\text{m}$  periphery FETs biased for minimum noise, with 50-ohm input and output beam-leaded rf ports. The transmitter

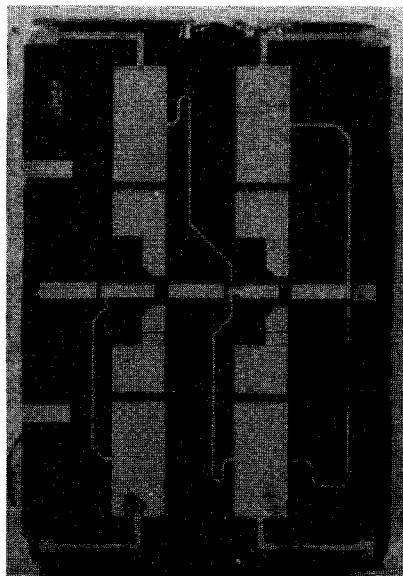


Fig. 3 Photograph of low-noise amplifier monolithic chip.

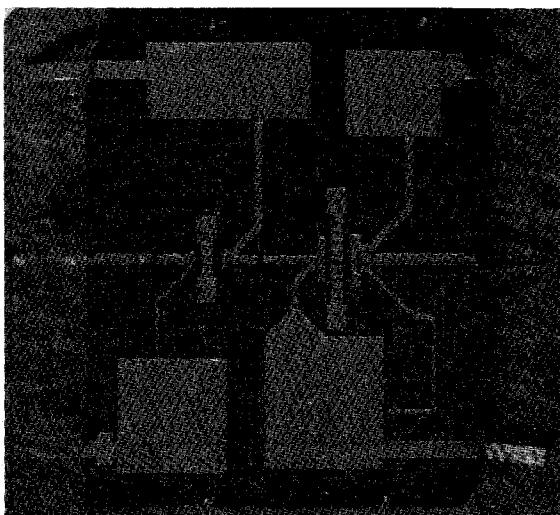


Fig. 4 Photograph of two-stage power amplifier monolithic chip.

also consists of two stages, the first a 600  $\mu\text{m}$  periphery FET driver and a 1600  $\mu\text{m}$  periphery "final" or power stage. The chip face dimensions are 2.5 and 3.2 mm. Here again, beam-leaded 50-ohm input and output ports are used for ease in testing. The module actually employs two identical transmitter circuits in cascade for more gain. In subsequent designs, all four stages will be redesigned and integrated into one chip. The phase-shifter consists of four cascaded "bits". Each bit contains a dual-gate FET with a "split" second gate and drain, and a common first gate. By appropriate control of the bias voltages on the two second gates, the amplified input signal can be made to exit one of two channels corresponding to either segment of the split drain. Each of the two channels is terminated on one of the two 3 dB ports of a Wilkinson combiner printed on the chip. The output of the bit appears at the remaining port the combiner. By introduction of an appropriate excess phase shift in one channel (produced by an additional microstrip line segment in one of the dual gate channels of each of the four chips), a differential phase shift can be obtained from each of the four phase-shifter chips. Because of the dual-gate FETs, each bit has some gain associated with it, that is, the phase-shifter is "active". The details of the phase-shifter design have been given elsewhere.<sup>3</sup>

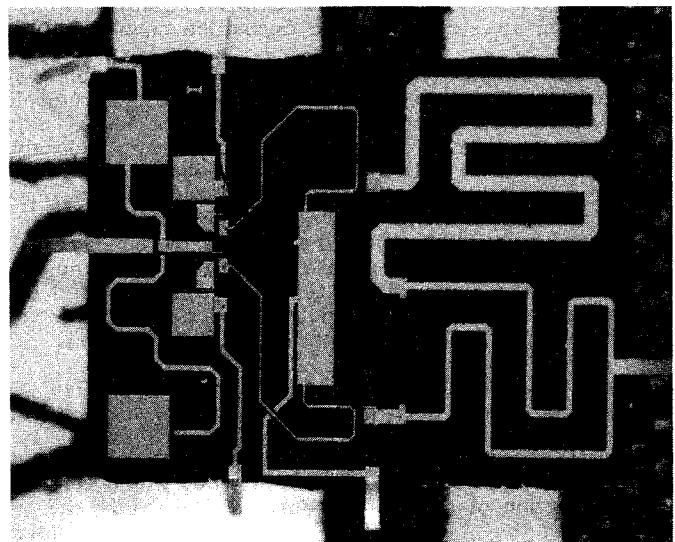


Fig. 5 Photograph of an active phase-shifter bit on monolithic form.

Figure 5 is a photograph of one of the four phase-shifter bits. Although the 100-ohm balancing resistor for the combiner is not visible, the two 90°-lines of the combiner, terminating in the common 50-ohm output port are clearly visible. The gate periphery of each FET channel is 140  $\mu\text{m}$ .

All of the chips described above use on-chip bias filtering consisting of thin-film capacitors which employ  $\text{Si}_3\text{N}_4$  dielectric films. Depending on the circuit, the capacitors range from 10 pF to 40 pF.

The switches use FETs in their resistive mode. Their design and operation have been described earlier.<sup>4</sup> Because the FETs are operated either at pinchoff, or at zero drain bias, no dc "hold" power is required in either state of the switch. This is a distinct advantage over PIN-type switches when minimization of dc prime power is important. The gate periphery of the FETs used is 1600  $\mu\text{m}$ . The chip face dimensions are 3.2 and 3.2 mm. Figure 6 is a photograph of a monolithic switch.

### Experimental Results Obtained with T/R Module

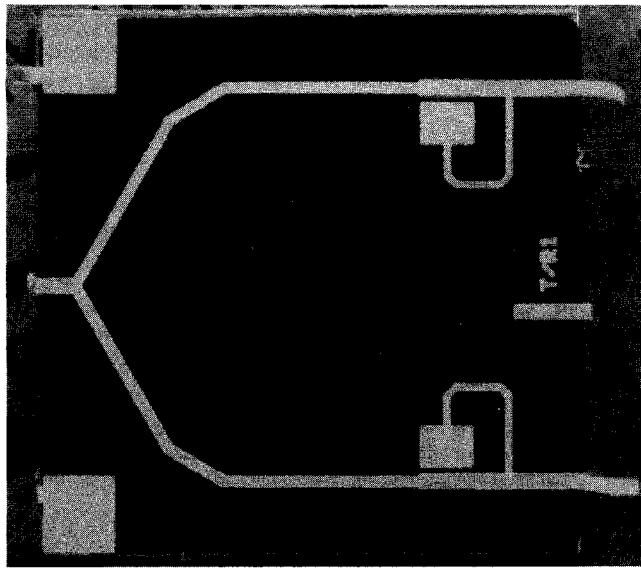


Fig. 6 Photograph of a monolithic FET switch.

Each of the monolithic chips was characterized individually after it was mounted on its carrier prior to installation in the T/R module housing. The assembled module was operated with gain over all 16 phase states, in both the receive and transmit modes.

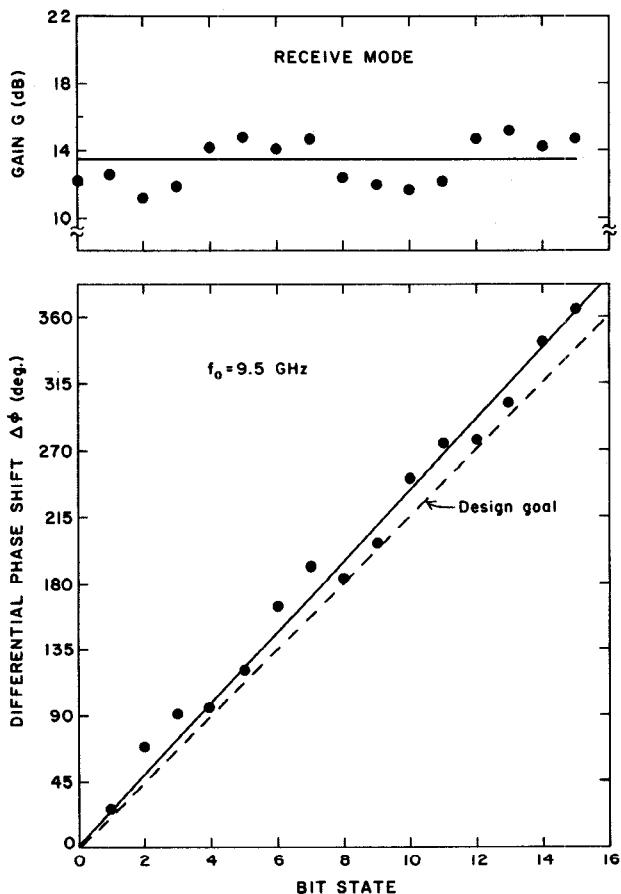


Fig. 7 Measured gain and differential phase shift at center band as a function of bit state (transmit mode).

Figure 7 displays the differential phase shift and gain in the transmit mode at the center band frequency  $f_0 = 9.5$  GHz. The median gain is 20 dB with a spread of approximately  $\pm 1.5$  dB. Actually, because the center band of the active phase-shifter, itself, was somewhat higher than the center-band frequency, a considerable gain slope occurred in the pass band. The phase-shift data exhibit an approximately linear variation with bit state, on the average, though the average slope is approximately 5% higher than the design specification. The saturated output power in the passband was approximately 250 mW.

Figure 8 illustrates the measured gain and phase response in the receive mode. The average gain is 13.6 dB with a variation of  $\pm 2$  dB over the bit states. The gain, of course, is lower than in the transmit mode because the low-noise amplifier has only two stages rather than four as in the transmitter. The phase-shift response is similar to the transmit mode as one would expect.

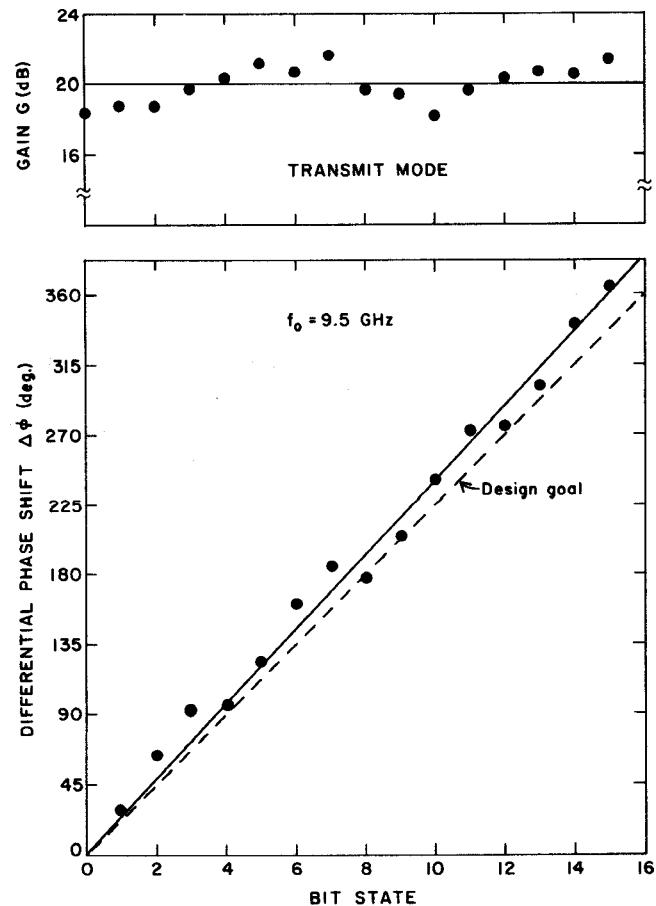


Fig. 8 Measured gain and differential phase shift at center band as a function of bit state (receive mode).

The noise figure in the receive mode was measured at selected points in the passband. The results are shown in Fig. 9. The spread in the data at each frequency (indicated by the vertical bars) reflects the variation in noise figure over the 16 bit states. These data were not corrected for fixture losses which are estimated, from independent measurements on the fixture itself, to be of the order of 0.25 dB. Contributing also to the noise figure is the antenna switch loss,

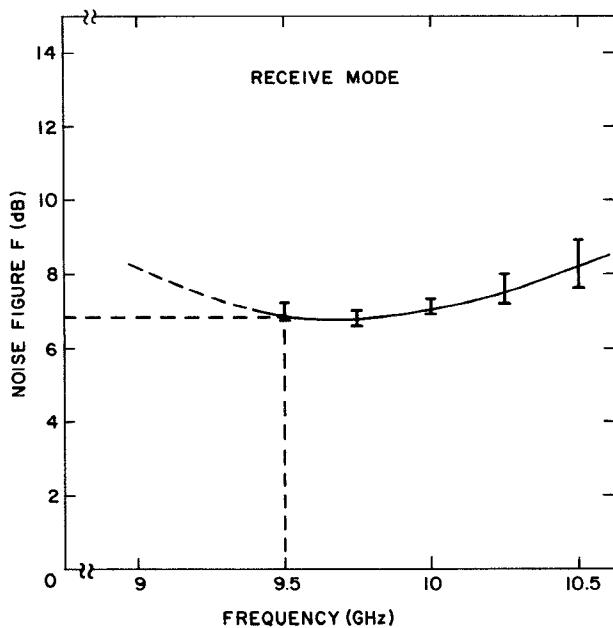


Fig. 9 Measured noise figure in receive mode as a function of frequency.

estimated to be 1.2 dB, and a microstrip loss on the alumina substrates of an amount equal to 0.15 dB. This leaves 5.2 dB at 9.5 GHz. Tests on the low-noise amplifier chip itself yield a noise figure of 5.0 dB (corrected for fixture losses). The difference in these two values is attributed to the noise figure of the active phase-shifter following the low-noise amplifier, inferred to be about 9 dB.

In this presentation, the philosophy underlying the module design will be covered in some detail. In

addition, a companion design, now under test, using a passive phase-shifter will be described, if results are available, and comparisons will be made between the two approaches.

#### Conclusions

We have shown that a transmit/receive module for phased-array antennas, based entirely on FET circuits, is technically feasible. Furthermore, a monolithic version of such a module (in multi-chip form) has exhibited promising performance for X-band applications. A salient feature of this design is the realization of an active phase-shifter, that is, one with gain.

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